A Novel Cascode Feedback GaAs MMIC LNA with Transformer-Coupled Output Using Multiple Fabrication Processes

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Abstract— **The design, development and performance of a novel high dynamic range cascode feedback GaAs MMIC LNA with transformer-coupled output is presented. The baseline design(chip size: 48 × 48 mils) operates over any 1 GHz bandwidth (with a simple off-chip input inductor) in the 0.5–3-GHz frequency range and has typically 15-dB small signal gain, 2.1-dB noise figure and greater than 15 dBm of output power at 1-dB gain compression point. Performance results of this circuit fabricated in three different foundry processes are also presented.**

I. Introduction

MOST of the reported low-frequency GaAs MMIC LNA's require two supply voltages and have low output power capability[1], [2]. Some MMIC LNA's have the output power capability at the expense of dc power(12 V, 120 mA) [3]. The MMIC LNA reported in this letter utilizes a novel single-stage cascode feedback design with transformer coupled output [4]. This circuit technique allows us to achieve low noise figure, good gain and high output power with low current consumption in a small chip size. The MMIC LNA operates from a single positive supply voltage.

II. Circuit Description And Performance

The circuit schematic of the single-stage GaAs MMIC cascode feedback LNA is shown in Fig. 1. The cascode configuration was used for two reasons[5], [6]: First, the cascode connected FET has much higher reverse isolation than a common source FET. The lower effective feedback capacitance (Miller Effect) allows greater bandwidth capability. Second, there is an improvement in output power capability since the output voltage swing is across the gate-drain junction of the common gate FET. In this case, the voltage swing may reach the gate-drain breakdown voltage of the device, while in the case of a common source device, it is limited by the gate-drain breakdown voltage less the negative voltage swing on the gate of the FET.

The RC feedback in this cascode circuit improves the S11 of the circuit and stabilizes the common gate FET without reducing the gain considerably and affecting the noise figure significantly. Due to the higher output impedance of the cascode configuration, a much higher feedback resistor (Rf > 700 ohm–1100 ohm, depending on the circuit version) can be used compared to 150–300 ohms in a conventional feedback amplifier design. This MMIC LNA has an off-chip input matching network such as a bondwire and spiral inductor on alumina which have higher Q than monolithic inductors on GaAs. This results in a highly versatile, unmatched LNA that can be tuned to achieve good input match and noise figure over a broad-band (any 1 GHz) in the 0.5–3-GHz frequency range.

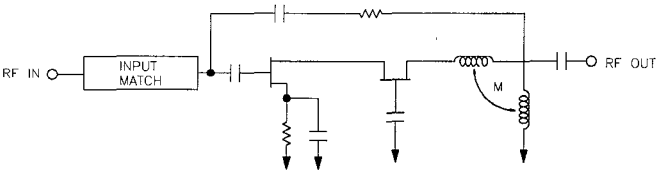

Fig. 1. Circuit schematic of a cascode feedback LNA with transformer coupled output.

A multiturn tapped spiral transformer is used at the output of the common gate FET to step down the high-impedance output of the common gate FET to 50 ohm. The output transformer also serves as a bias choke for supplying the dc voltage to the device. A voltage divider is used to bias the gate of the common gate FET while the common source FET is self-biased through a source resistor. Both the input and output of the circuit have dc blocks.

This cascode feedback MMIC LNA has been designed and fabricated using three different MMIC processes. The baseline design was done using Triquint's HA process (Process A). FET widths of 1 mm (biased at 20% Idss, 6 V to 8 V @ 27 mA) were used. Fig. 2 shows the photograph of the assembled chip (48 mils × 48 mils). The simulated gain and noise figure of this chip were 15 dB and 2 dB, respectively. Small signal gain, input and output return loss performance of this chip in a surface mount package (170 mils × 170 mils, with input matching inductor and dc bypassed capacitor) are depicted in Fig. 3 for an input matching of 1 GHz–3 GHz. The measured gain variation over temperature (−55°C to +85°C) was ± 0.6 dB. The two-tone third-order intermodulation products measured at 1 GHz are 54.41 dBc and the third-order intercept point is 27.35 dBm.

Another version of this amplifier has been designed for even lower dc power consumption (5v @ 22 mA) and smaller

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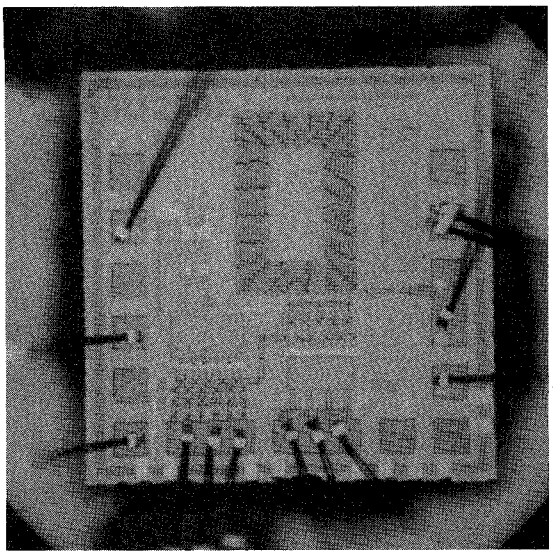

Fig. 2. Photograph of the assembled cascode feedback MMIC LNA (chip size: 48 mils × 48 mils).

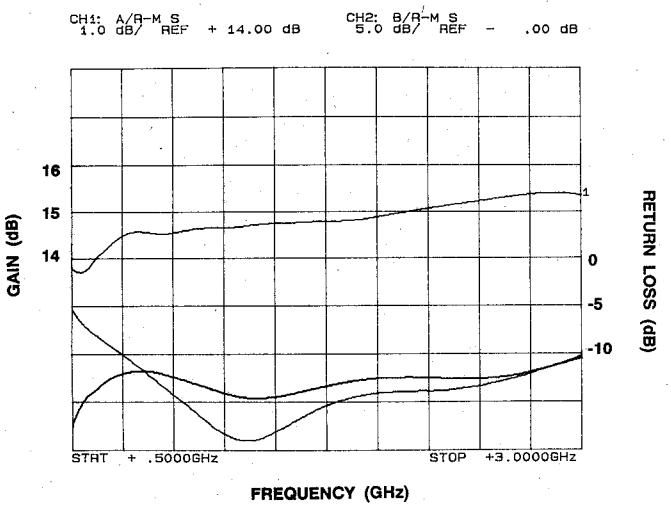

Fig. 3. Gain and return loss performance of the cascode feedback MMIC LNA in a package.

chip size (36 mils × 36 mils) using an E/D (Enhancement/Depletion) GaAs MMIC process (Process C). Using FET's with two different pinch-off voltages, it was possible to ground the FET's directly, eliminating the RF bypass capacitors and reduce chip size. A FET size of 1 × 500 micron was used in this version. A photograph of the assembled chip is shown in Fig. 4. Simulated and measured small signal gain and output power were 2.5 dB lower than the baseline version.

A third version of the baseline design using 0.5 × 1000 micron depletion mode FET's was fabricated using a low noise ion-implanted process. This low-noise process has a factor of 2 lower source resistance and 0.9-V pinch-off (Process B). This version showed improved noise figure and gain performance both in simulation (1.7 dB and 16.5 dB, respectively) and in measurement. The performance summary of all these amplifier

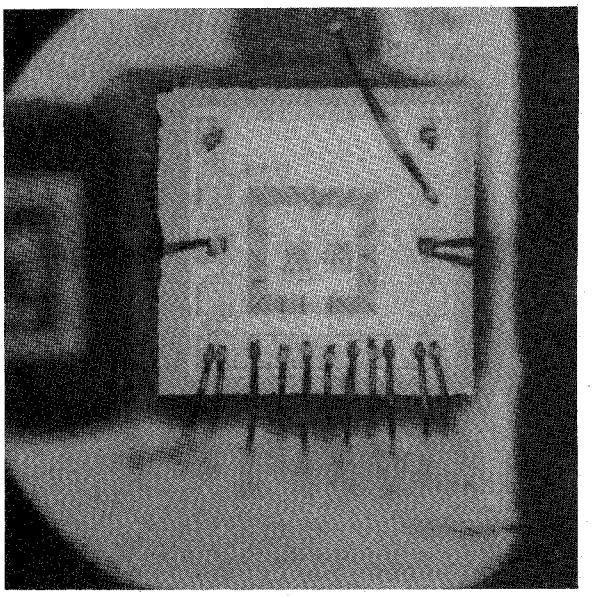

Fig. 4. Photograph of the assembled cascode feedback MMIC LNA using E/D process (chip size: 36 mils × 36 mils).

TABLE I
CASCODE FEEDBACK GaAs MMIC LNA WITH TRANSFORMER-COUPLED OUTPUT

Parameters	GaAs MMIC Processes		
	A	B	C
FET Size (μm)	0.5 × 1000	0.5 × 1000	1 × 500
Freq. (GHz)	0.5 – 3.0	0.5 – 3.0	0.5 – 3.0
S.S. Gain (dB)	14.5	16	12
Input VSWR	1.6:1	1.6:1	1.6:1
Output VSWR	1.6:1	1.6:1	1.6:1
P-1 dB (dBm)	15.5	16	12
N.F. (dB)	2.0	1.8	2.2
OIP3 (dBm)	25	26	22
dc Voltage (V)	6V to 8V	6V to 8V	5V to 8V
dc Current (mA)	27	28	22
Chip Size (mils)	48 × 48	48 × 48	36 × 36

*Typical performance summary for three different processes.

versions fabricated in different processes are shown in Table I. All of these different versions have been used in the design of subsystems below 3 GHz [7], [8] and a variation of the baseline design approach has also been successfully tested in the 5–6-GHz range.

III. CONCLUSION

A novel cascode feedback MMIC LNA with transformer-coupled output has demonstrated good gain, noise figure, return loss and output power capability. The baseline design approach has also been successfully fabricated and tested in three different MMIC fabrication processes with comparable performance.

ACKNOWLEDGMENT

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